DS21610
Clock Rate Adapter

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FEATURES

- Direct replacement for LXP610SE
- Converts E-carrier clock rates to T-carrier clock rates
- Converts T-carrier clock rates to E-carrier clock rates
- Low-output jitter
- Multiple output clocks synchronized to input clock
- 8kHz frequency-locked output for all modes of operation
- No external components required
- 16-pin SO and 28-pin PLCC
- Industrial temperature range: -40ºC to +85ºC

ORDERING INFORMATION

DS21610SN	16-pin SO	-40°C to +85°C
DS21610QN	28-pin PLCC	-40°C to +85°C

DESCRIPTION

The DS21610 is a multi-rate, low-jitter clock adapter that converts E-carrier and T-carrier clocks to multiple PDH carrier clock rates. Two clock outputs are available that are frequency-locked to the input clock. The clock outputs along with an 8kHz frame sync output can be phased aligned to a frame sync input. The device is backward compatible to the LXP610 and operates from a single 5V supply. All modes of operation include a standard 8kHz output.

TABLE OF CONTENTS

LIST OF TABLES

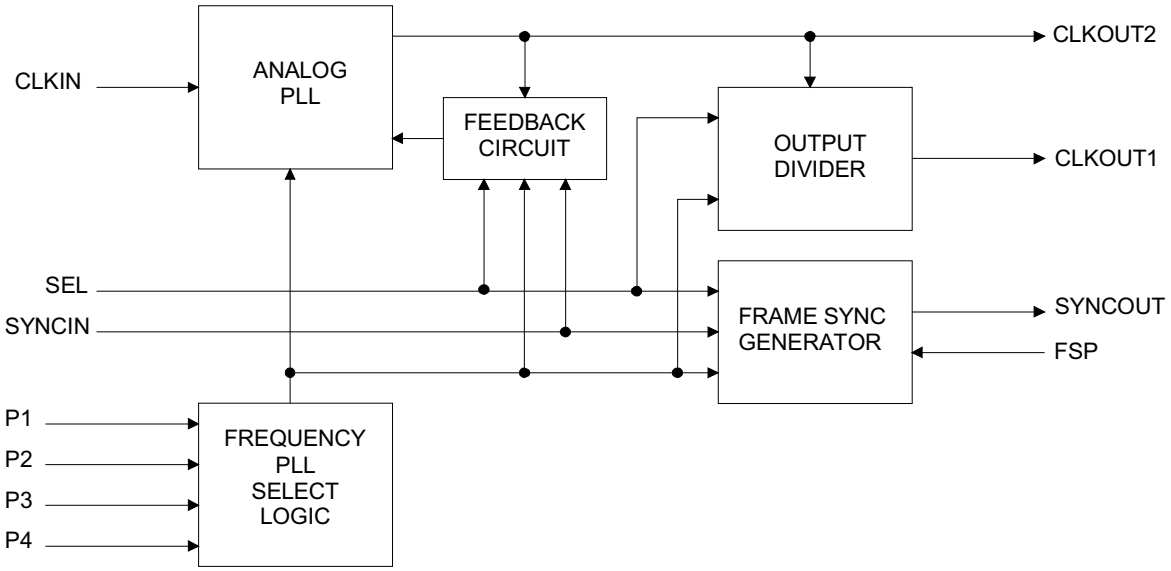
LIST OF FIGURES

1. FUNCTIONAL DESCRIPTION

A clock input at CLKIN is converted to various clocks available on CLKOUT1 and CLKOUT2. Additionally, an 8kHz clock locked to CLKIN and SYNCIN (if present) is always available at the SYNCOUT pin. The pulse width of the SYNCOUT is selectable. It can be one or one-half the clock period of CLKIN, centered on the rising edge of CLKIN. Pins P1–P4 are used to select the various clock rates and operational modes. Table 2-1 and Table 2-2 lists the various operational modes of the DS21610.

CLKIN, CLKOUT1, and CLCKOUT2 are always frequency-locked. They can all be phase-locked to a system frame-sync pulse. A frame-sync pulse applied to SYNCIN will cause CLKIN and CLKOUT1 and CLKOUT2 to be phased-locked to that sync pulse. This will cause the clocks to have a fixed alignment at the frame-sync boundaries. The signal applied to SYNCIN can be 8kHz or some integer subrate such as 1kHz, 2kHz, or 4kHz. Phase synchronization will occur within a maximum of 50ms when SYNCIN is 8kHz.

DS21610 BLOCK DIAGRAM Figure 1-1



1.1 PIN FUNCTION DESCRIPTION

Signal Name: CLKIN
Signal Description: **Clock Input**
Signal Type: **Input**
Reference Clock Input. CLKOUT1 and CLKOUT2 will be referenced to this clock.

Signal Name: CLKOUT1
Signal Description: **Clock Output 1**
Signal Type: **Output**
T1 or E1 carrier clock output referenced to CLKIN.

Signal Name: CLKOUT2
Signal Description: **Clock Output 2**
Signal Type: **Output**
T1 or E1 carrier clock output referenced to CLKIN.

Signal Name: P1 to P4
Signal Description: **Program Pins 1 – 4**
Signal Type: **Input**
Used to select the various combinations of clock and sync outputs.

Signal Name: SEL
Signal Description: **Clock Mode Select**
Signal Type: **Output**
T-carrier/E-carrier mode select.

Signal Name: SYNCIN
Signal Description: **Synchronization Input**
Signal Type: **Input**
Used to synchronize the clock outputs and SYNCOUT to CLKIN and SYNCIN.

Signal Name: SYNCOUT
Signal Description: **Synchronization Output**
Signal Type: **Output**
An 8kHz output that will be synchronized to the clock outputs and SYNCIN (if present).

Signal Name: FSP
Signal Description: **Frame Synchronization Pulse Polarity**
Signal Type: **Input**
Used to change the polarity of the SYNCOUT output.

Signal Name: V_{DD}
Signal Description: **Positive Supply**
Signal Type: **Supply**
5V ±5%

Signal Name: V_{ss}
Signal Description: **Signal Ground**
Signal Type: **Supply**
Ground

PIN DESCRIPTION SORTED BY PIN NUMBER Table 1-1

28-PIN PLCC PIN #	16-PIN SO PIN #	PIN NAME	TYPE	DESCRIPTION
1	1	P3	I	Program Pin 3
2	2	SYNCOUT	O	Synchronization Pulse Output
3	3	N/C	-	NO CONNECT
4	-	N/C	-	NO CONNECT
5	-	N/C	-	NO CONNECT
6	4	CLKOUT2	O	Clock 2 Output
7	-	N/C	-	NO CONNECT
8	-	N/C	-	NO CONNECT
9	-	N/C	-	NO CONNECT
10	5	CLKIN	I	Clock Input
11	6	N/C	-	NO CONNECT
12	-	N/C	-	NO CONNECT
13	7	CLKOUT1	O	Clock 1 Output
14	8	P1	I	Program Pin 1
15	9	V_{SS}	-	Ground
16	10	P2	I	Program Pin 2
17	-	N/C	-	NO CONNECT
18	-	N/C	-	NO CONNECT
19	11	N/C	-	NO CONNECT
20	12	SEL	I	Clock Mode Select
21	-	N/C	-	NO CONNECT
22	13	FSP	I	Frame Sync Polarity
23	-	N/C	-	NO CONNECT
24	14	SYNCIN	I	Synchronization Pulse Input
25	-	N/C	-	NO CONNECT
26	-	N/C	-	NO CONNECT
27	15	P4	I	Program Pin 4
28	16	V_{DD}	-	Positive Supply

1.2 COMPATIBLITY TO LXP610

The DS21610 is pin-compatible to the LXP610.

PIN NAME CROSS-REFERENCE TO LXP610 Table 1-2

DS21610 PIN NAME	LXP610 PIN NAME	DESCRIPTION
P3	P3	Program Pin 3
SYNCOUT	FSO	Synchronization Pulse Output
CLKOUT2	HFO	Clock 2 Output
CLKIN	CLKI	Clock Input
CLKOUT1	CLKO	Clock 1 Output
P1	P1	Program pin 1
V_{SS}	GND	Ground
P2	P2	Program Pin 2
N/C	N/C	NO CONNECT
SEL	SEL	Clock Mode Select
FSP	FSP	Frame Sync Polarity
SYNCIN	FSI	Synchronization Pulse Input
P4	P4	Program Pin 4
V_{DD}	V_{CC}	Positive Supply

2. OPERATION

PROGRAM PIN FUNCTIONS (SEL = 0) Table 2-1

P4	P3	P2	P1	CLKIN	CLKOUT1	CLKOUT2	SYNCOUT
0	0	0	0	1.544	2.048	6.144	LONG
0	0	0	1	3.088	2.048	8.192	SHORT
0	0	1	0	1.544	2.048	6.144	LONG
0	0	1	1	1.544	2.048	8.192	SHORT
0	1	0	0	1.544	2.560	7.680	LONG
0	1	0	1	6.176	4.096	8.192	LONG
0	1	1	0	1.544	2.560	7.680	LONG
0	1	1	1	6.176	2.048	8.192	SHORT
1	0	0	0	3.088	2.048	6.144	LONG
1	0	0	1	3.088	4.096	8.192	LONG
1	0	1	0	3.088	2.048	6.144	LONG
1	0	1	1	1.544	4.096	8.192	LONG
1	1	0	0	6.176	2.560	7.680	LONG
1	1	0	1	6.176	4.096	8.192	LONG
1	1	1	0	6.176	2.560	7.680	LONG
1	1	1	1	6.176	4.096	8.192	LONG

PROGRAM PIN FUNCTIONS (SEL = 1) Table 2-2

P4	P3	P2	P1	CLKIN	CLKOUT1	CLKOUT2	SYNCOUT
0	0	0	0	2.048	3.088	6.176	LONG
0	0	0	1	2.048	3.088	6.176	LONG
0	0	1	0	2.048	1.544	6.176	LONG
0	0	1	1	2.048	1.544	6.176	LONG
0	1	0	0	2.560	1.544	7.720	LONG
0	1	0	1	8.192	3.088	6.176	LONG
0	1	1	0	2.560	1.544	7.720	LONG
0	1	1	1	8.192	1.544	6.176	LONG
1	0	0	0	2.048	3.088	6.176	LONG
1	0	0	1	4.096	3.088	6.176	LONG
1	0	1	0	2.048	3.088	6.176	LONG
1	0	1	1	4.096	1.544	6.176	LONG
1	1	0	0	2.560	1.544	7.720	LONG
1	1	0	1	8.192	3.088	6.176	LONG
1	1	1	0	2.560	1.544	7.720	LONG
1	1	1	1	8.192	1.544	6.176	LONG

3. JITTER SPECIFICATIONS

OUTPUT JITTER SPECIFICATIONS, CLKOUT1 = 1.544MHz Table 3-1

FREQUENCY BAND	TR62411 SPECIFICATION	TYP	MAX	UNIT
No Bandlimiting	0.050	0.002	0.020	UIpp
10Hz to 40kHz	0.025	0.001	0.010	UIpp
8kHz to 40kHz	0.025	0.001	0.012	UIpp

Note: CLKIN = 2.048MHz OR 4.096MHz

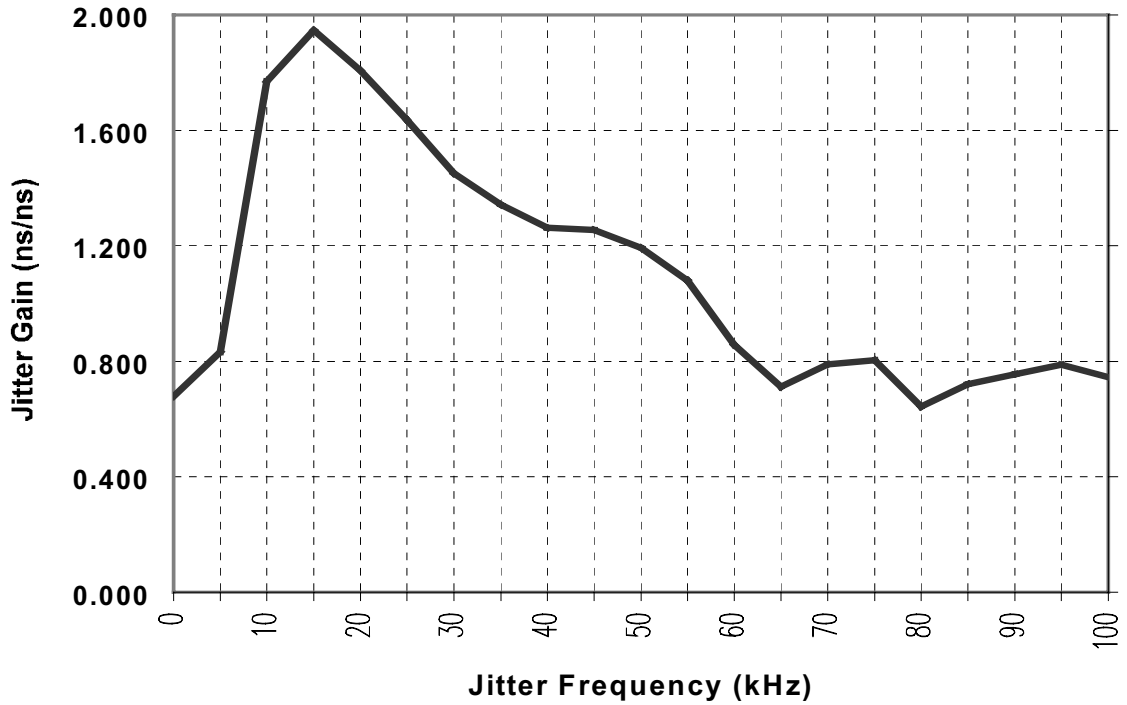
OUTPUT JITTER SPECIFICATIONS, CLKOUT1 = 2.048MHz Table 3-2

FREQUENCY BAND	G.823 SPECIFICATION	TYP	MAX	UNIT
20Hz to 100kHz	1.5	0.012	0.035	UIpp
18kHz to 100kHz	0.2	0.008	0.025	UIpp

Note: CLKIN = 1.544MHz

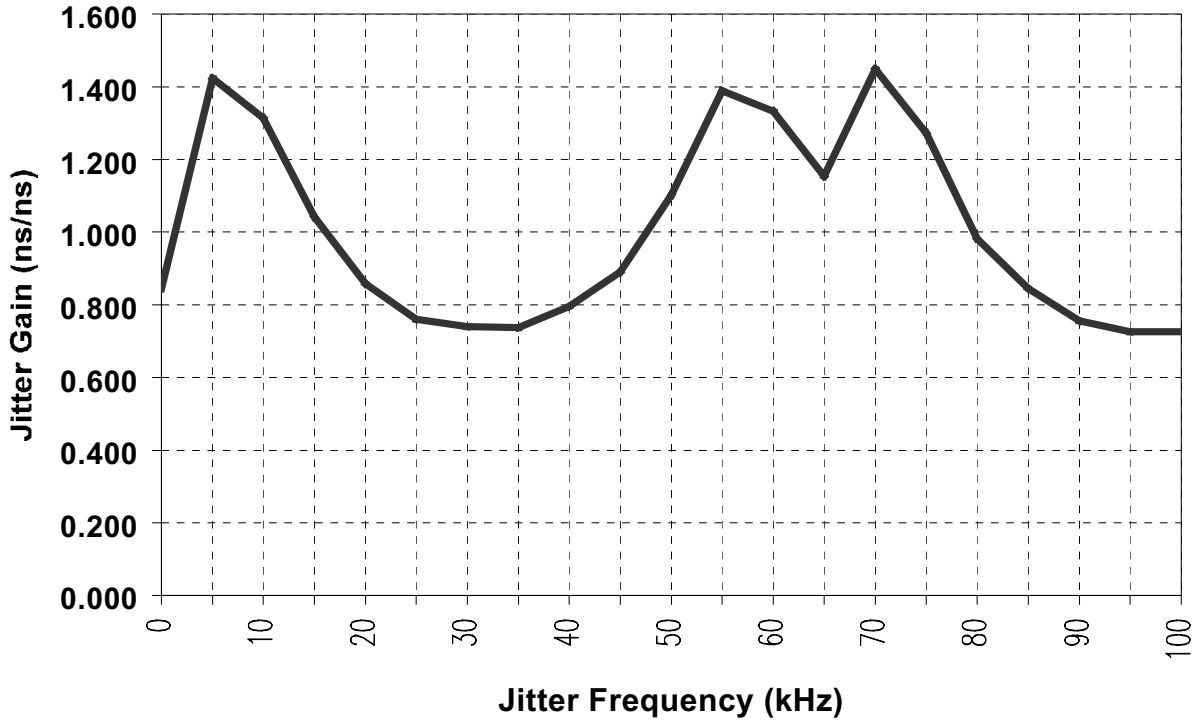
NOMINAL JITTER TRANSFER (1.544MHz CLKIN to 2.048MHz CLKOUT1)

Figure 3-1



NOMINAL JITTER TRANSFER (2.048MHz CLKIN to 1.544MHz CLKOUT1)

Figure 3-2



4. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS*

Voltage Range on Any Pin Relative to Ground	-1.0V to +6.0V
Operating Temperature Range for DS21610SN	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		5.5	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply for 5V Operation	V_{DD}	4.75	5	5.25	V	

DC CHARACTERISTICS (-40°C to +85°C; V_{DD} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}			8	mA	2
Input Leakage	I_{IL}	-10.0		+10.0	µA	1
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. $0.0V < V_{IN} < V_{DD}$.
2. Outputs open.

4.1 TIMING

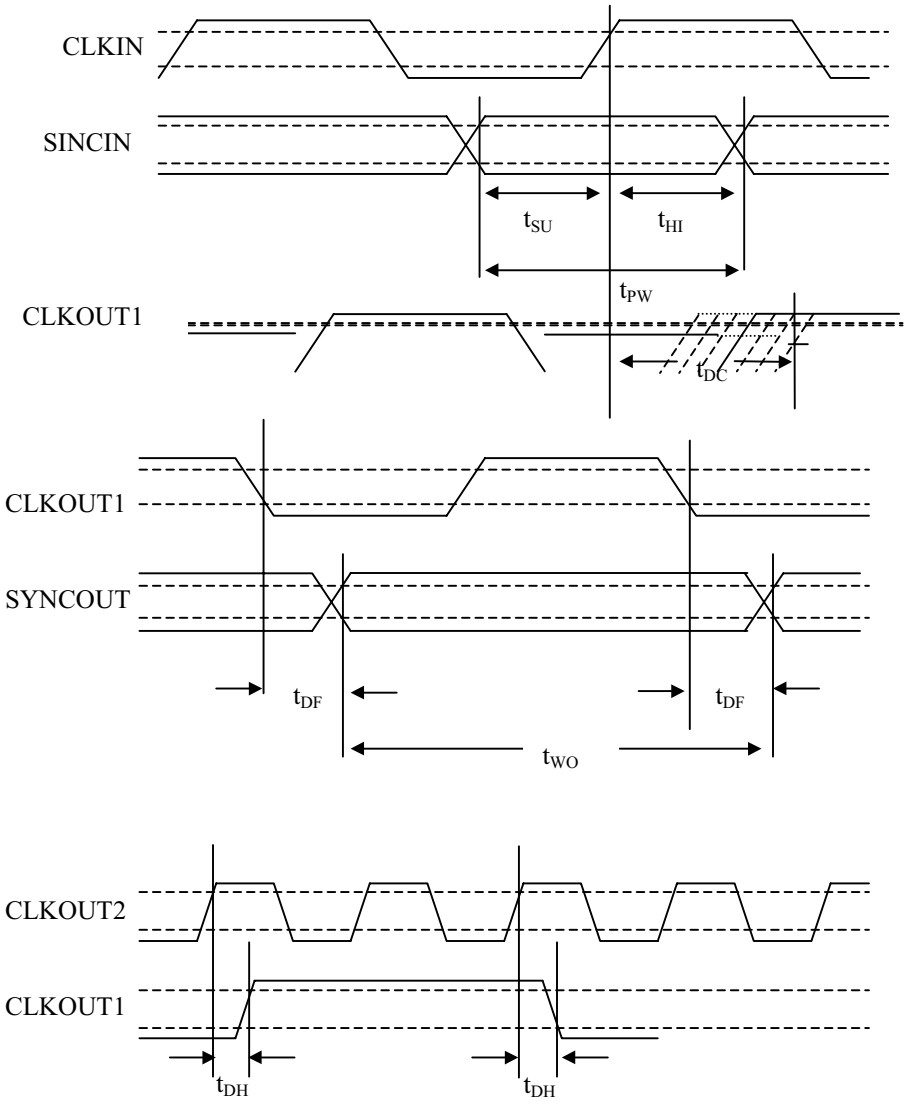
AC TIMING Table 4-1

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Capture Range on CLKIN[1]		±10000	-	-	ppm
Lock Range on CLKIN[1]		±10000	-	-	ppm
CLKIN Duty Cycle[1]		35	-	65	%
SYNCIN Setup to CLKIN Rising	t_{SU}	46	-	-	ns
SYNCIN Hold After CLKIN Rising	t_{HI}	30	-	-	ns
SYNCIN Pulse Width	t_{PW}	76		CLKIN period	ns
CLKOUT1 Delay From CLKIN Rising	t_D	-15	0	+15	ns
CLKOUT1 Duty Cycle	C_D	49	-	51	%
SYNCOUT Delay From CLKOUT2	t_{DF}	-5	-	30	ns
SYNCOUT Pulse Width (Low)	t_{SPW}	-	-	CLKOUT1 Period	ns
CLKOUT1 Delay From CLKOUT2 Rising	t_{DH}	-15	0	+15	ns
Rise/Fall Time on CLKIN, SYNCIN[1]	t_{RF}	-	-	40	ns
Rise/Fall Time on CLKOUT, SYNCOUT, CLKOUT2 with a 26pF load	t_{RF}	-	-	40	ns

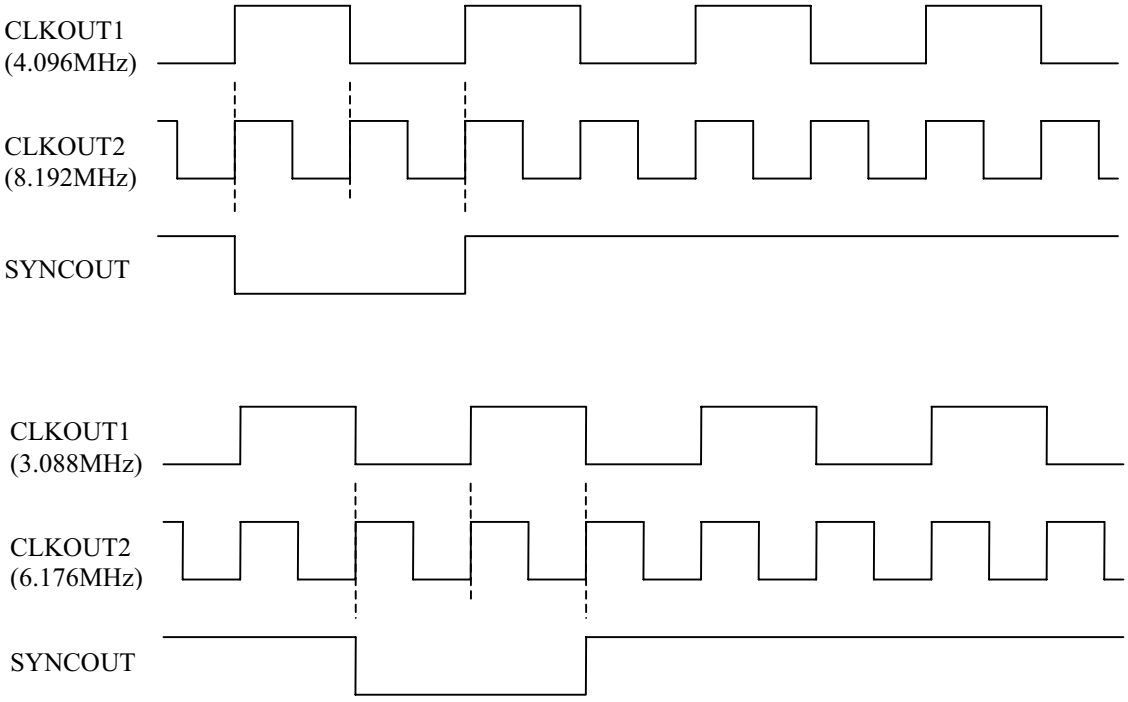
1. Guaranteed by design

AC TIMING DIAGRAMS Figure 4-1

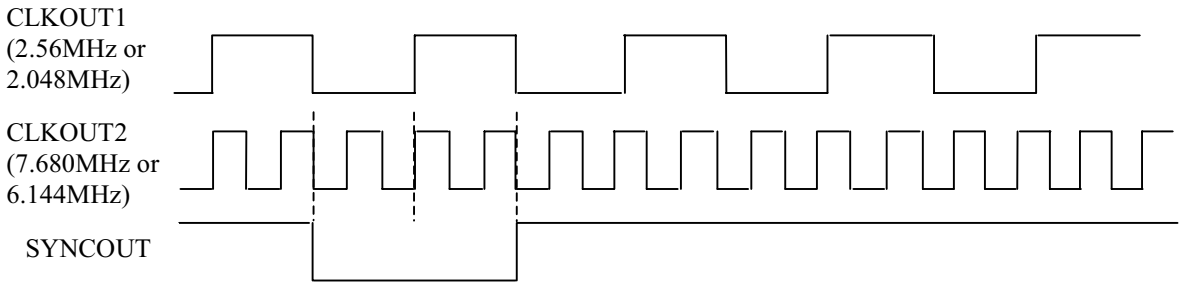
SYNCIN/CLKIN to CLKOUT1/SYNCOUT and CLKOUT2



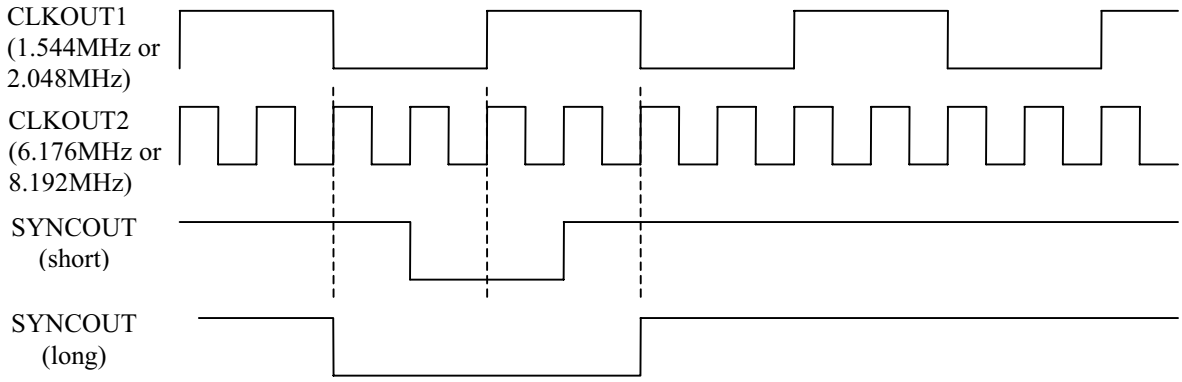
Output Frame Sync Alignment When CLKOUT2 = 2 x CLKOUT1



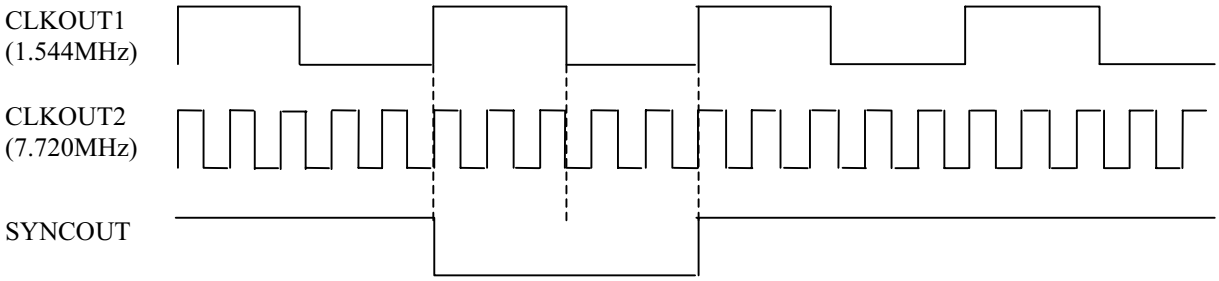
Output Frame Sync Alignment When CLKOUT2 = 3 x CLKOUT1



Output Frame Sync Alignment When CLKOUT2 = 4 x CLKOUT1

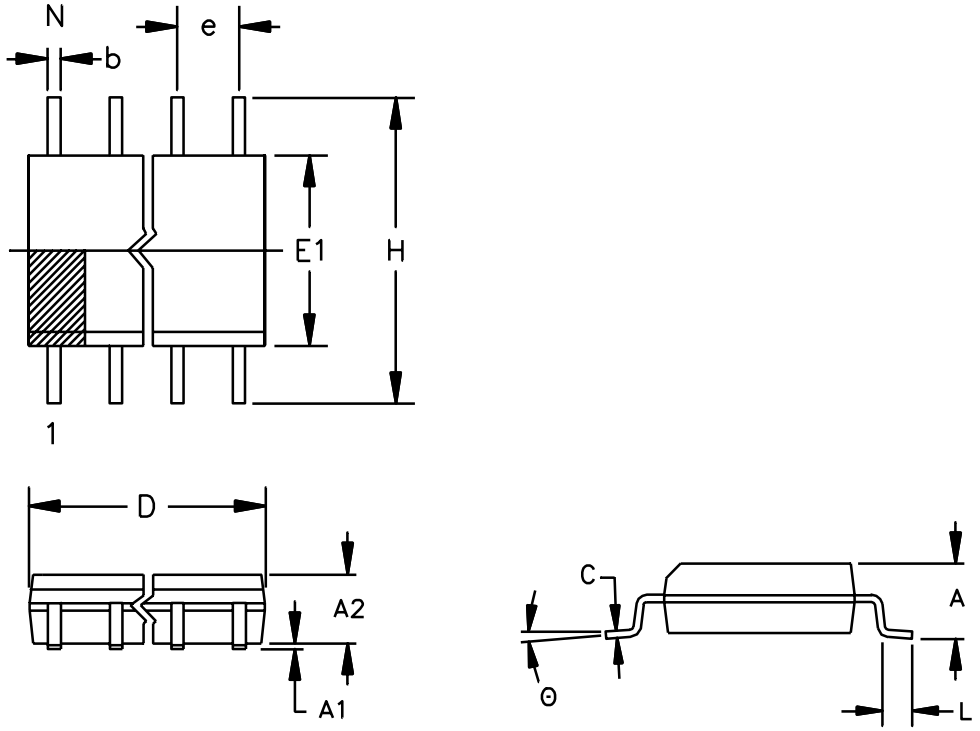


Output Frame Sync Alignment When CLKOUT2 = 5 x CLKOUT1



5. PACKAGE SPECIFICATIONS

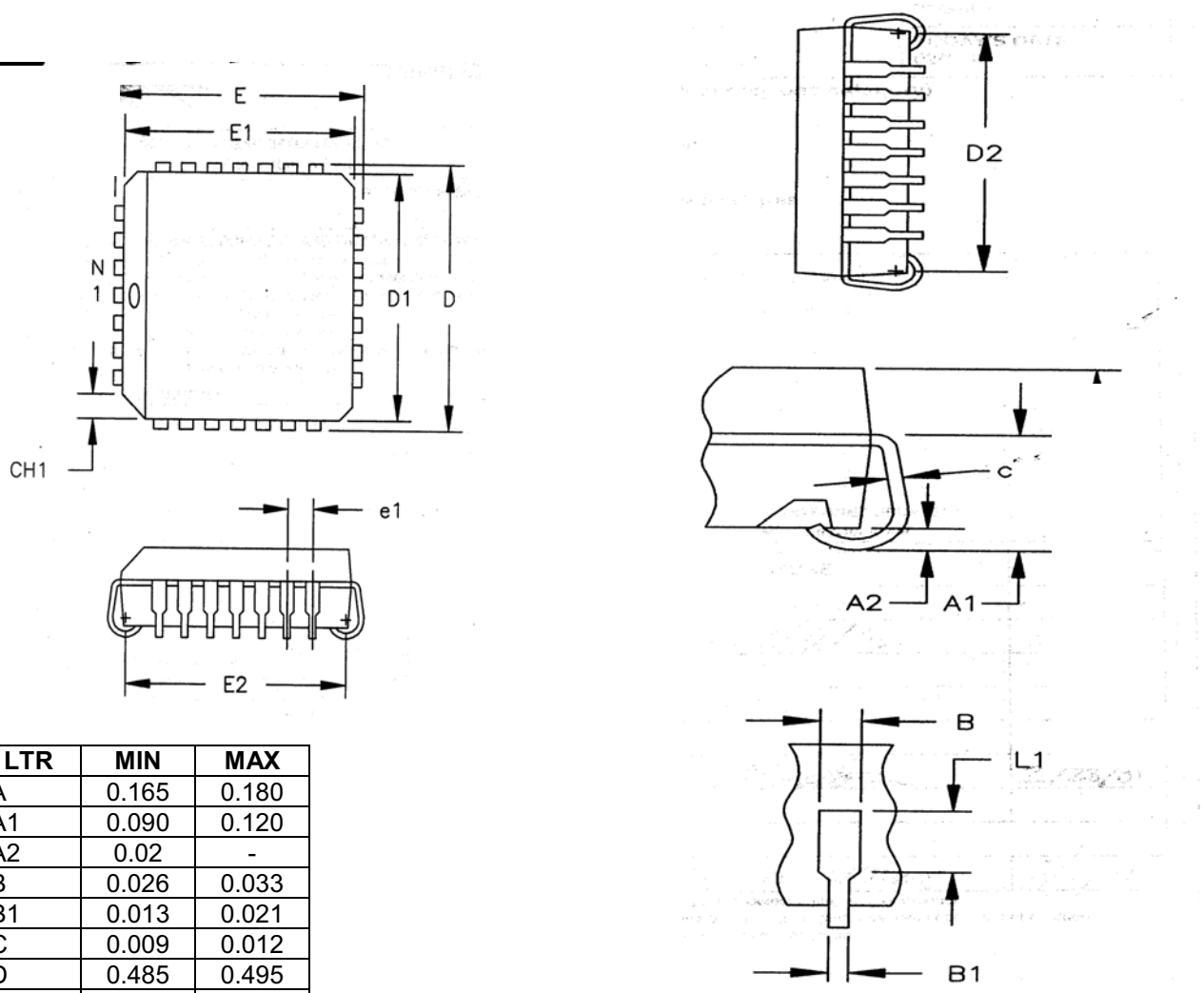
PACKAGE OUTLINE SO 16-PIN 0.300″ BODY Figure 5-1



LTR		MIN	MAX
A	IN.	0.094	0.105
	MM	2.39	2.67
A1	IN.	0.004	0.012
	MM	0.102	0.30
A2	IN.	0.089	0.095
	MM	2.26	2.41
b	IN.	0.013	0.020
	MM	0.33	0.51
C	IN.	0.009	0.013
	MM	0.229	0.33
D	IN.	0.398	0.412
	MM	10.11	10.46
e	IN.	.050 BSC	
	MM	1.27 BSC	
E1	IN.	0.290	0.300
	MM	7.37	7.62
H	IN.	0.398	0.416
	MM	10.11	10.57
L	IN.	0.016	0.040
	MM	0.40	1.02
Θ		0°	8°

THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A TERMINAL 1 IDENTIFIER MUST BE POSITIONED IN THE HATCHED ZONE.

PACKAGE OUTLINE PLCC 28-PIN PACKAGE Figure 5-2



LTR	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.02	-
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	-
N	28	-
E1	0.050	BSC
Ch1	0.042	0.048

6. REVISION HISTORY

1. Preliminary release, 090100.
2. Remove references to 3V operation, 112700.
3. Add FSP pin to block diagram, 120600.
4. Add mechanical drawings for PLCC package, 021501.
5. Added jitter specifications and pinout for all packages, 060601.
6. Added timing diagrams, 082001.